6715020

FIG_1

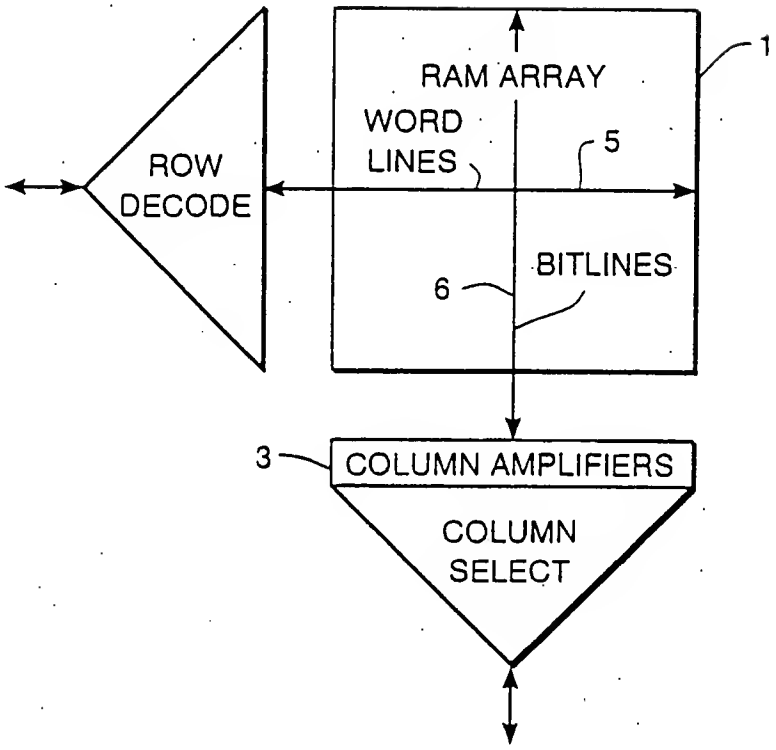

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FIG_2

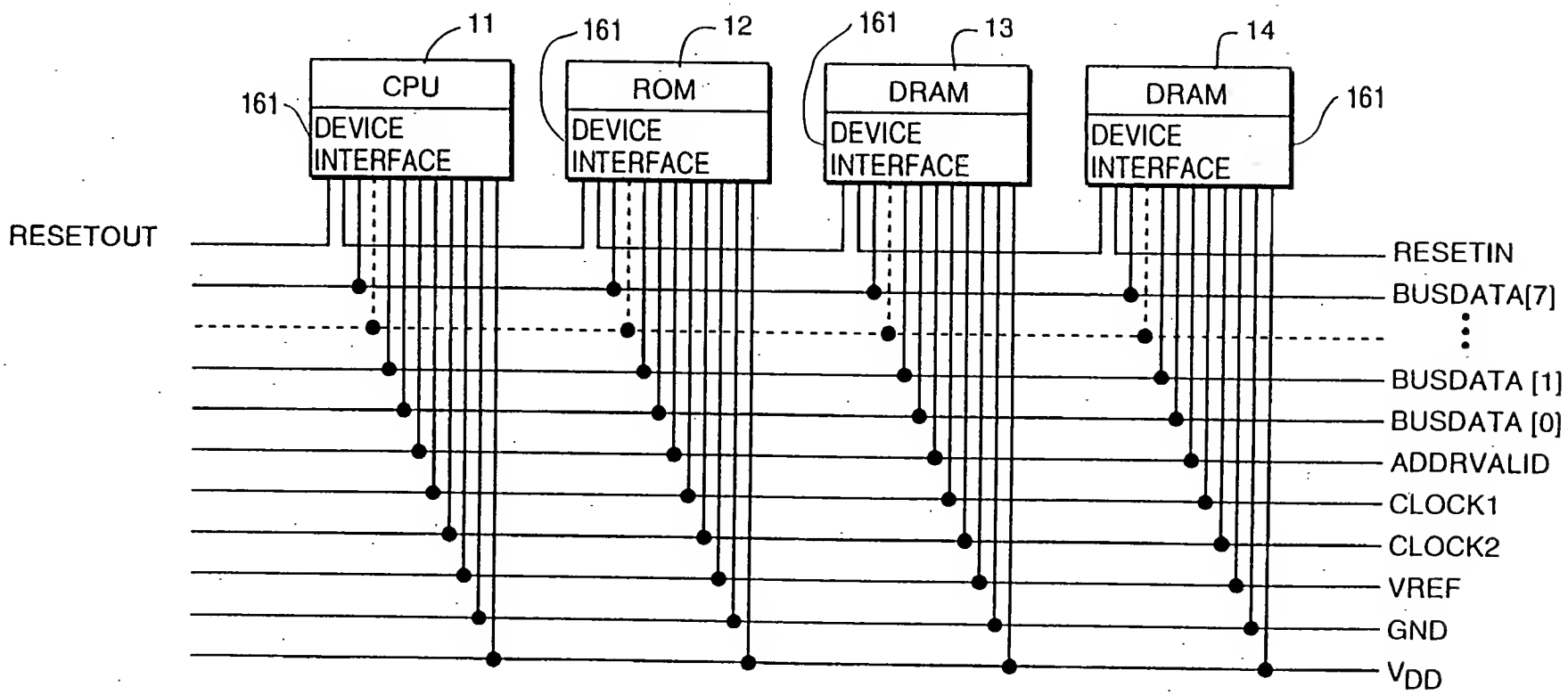
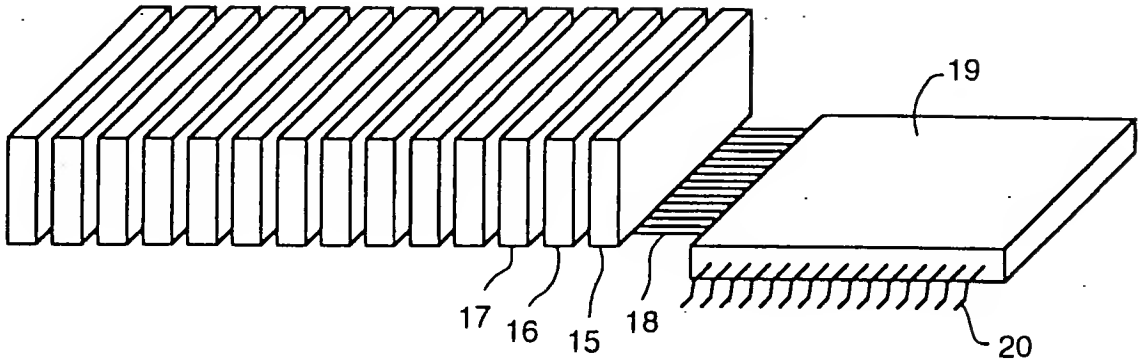

11
161
12
161
13
14
161
161
CPU
ROM
DRAM
DRAM
DEVICE INTERFACE
DEVICE INTERFACE
DEVICE INTERFACE
DEVICE INTERFACE
RESETOUT
RESETIN
BUSDATA[7]
BUSDATA [1]
BUSDATA [0]
ADDRVALID
CLOCK1
CLOCK2
VREF
GND
V_{DD}

FIG_3



REGULAR ACCESS

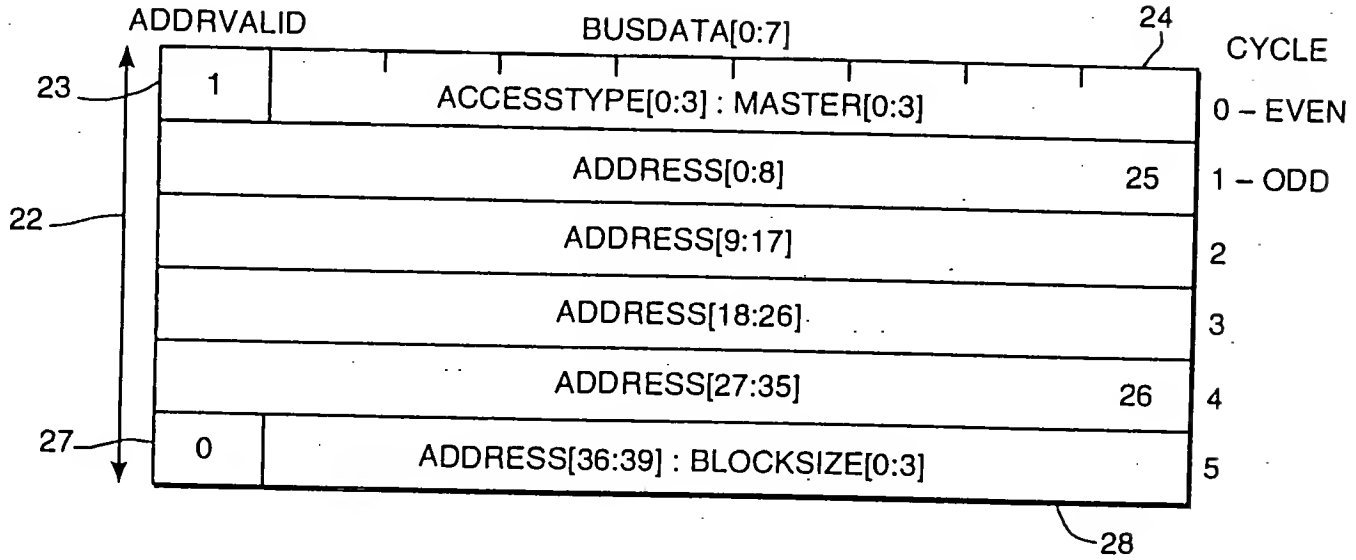


FIG_4

REJECT (NACK) CONTROL PACKET

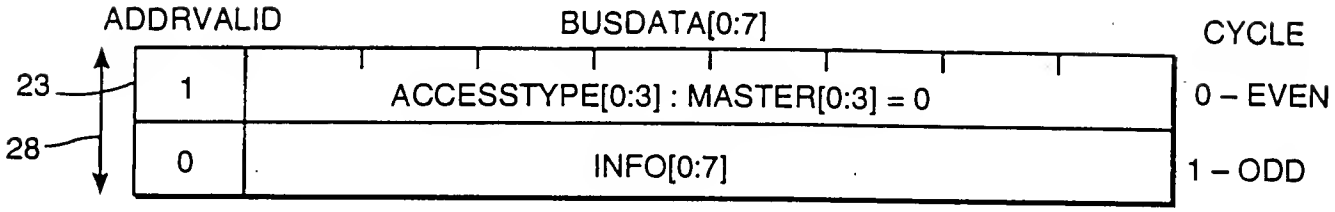


FIG_5

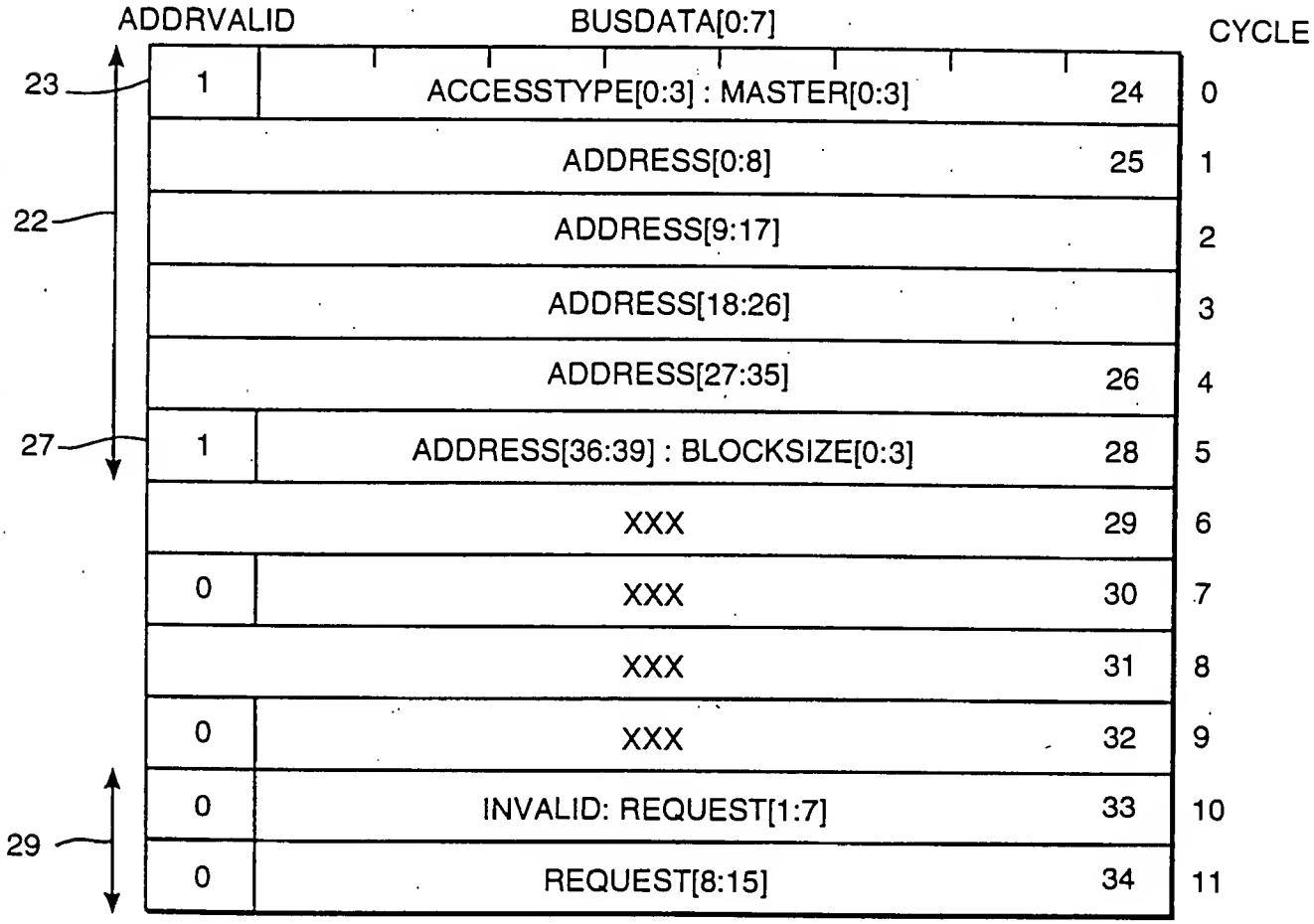


FIG_6

EP 1 227 704 A2

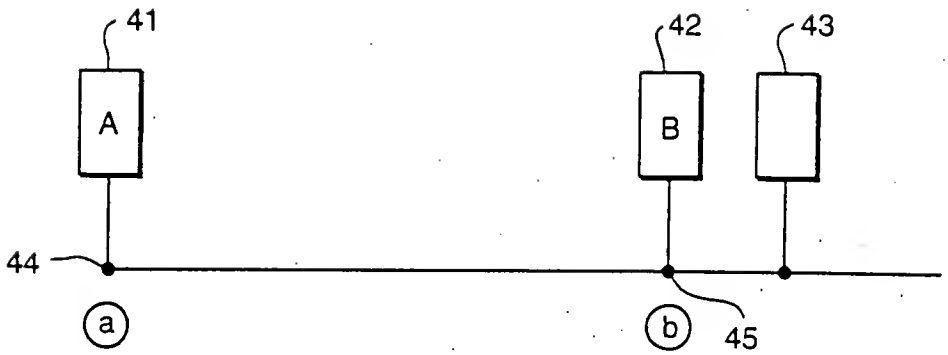


FIG_7A

FOR2F' F7F7E00F

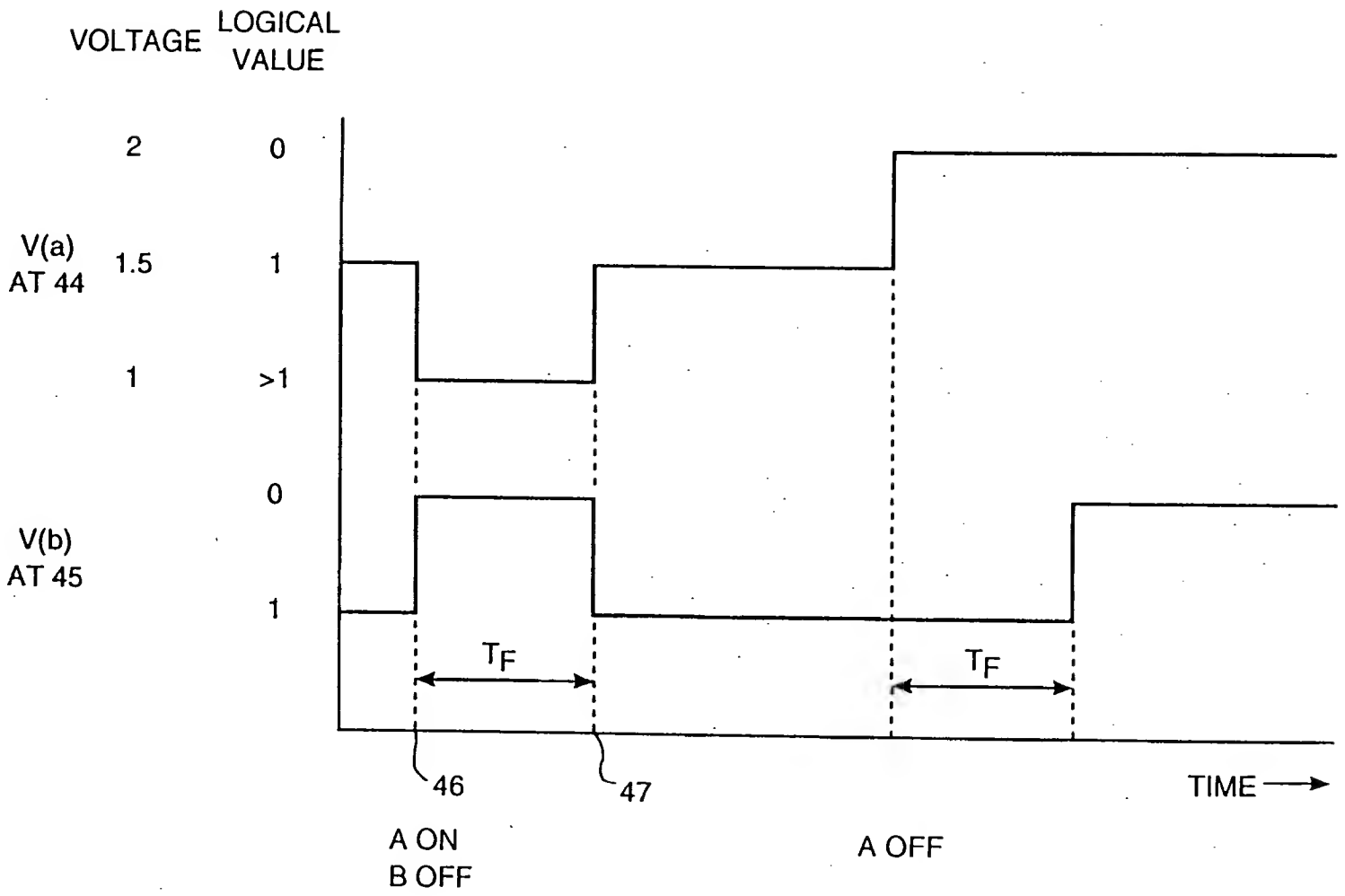


FIG_7B

FOREST-F-N3605

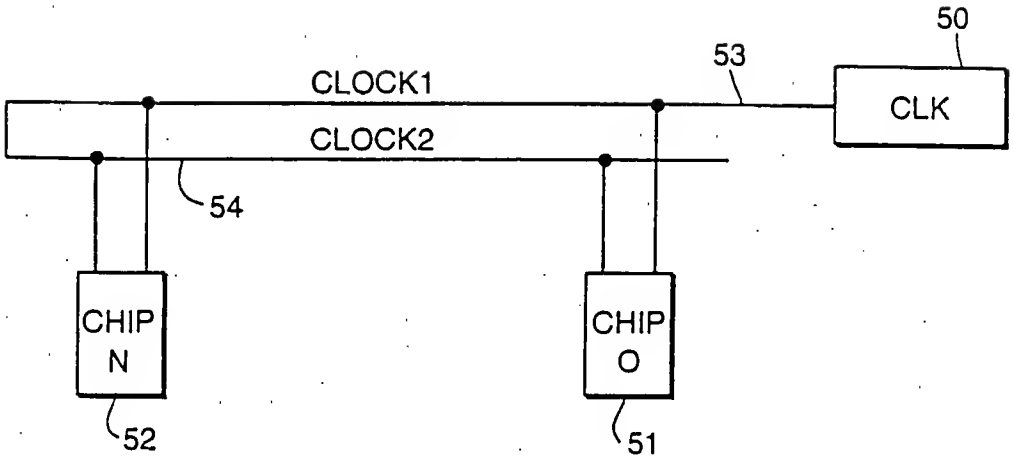


FIG_8A

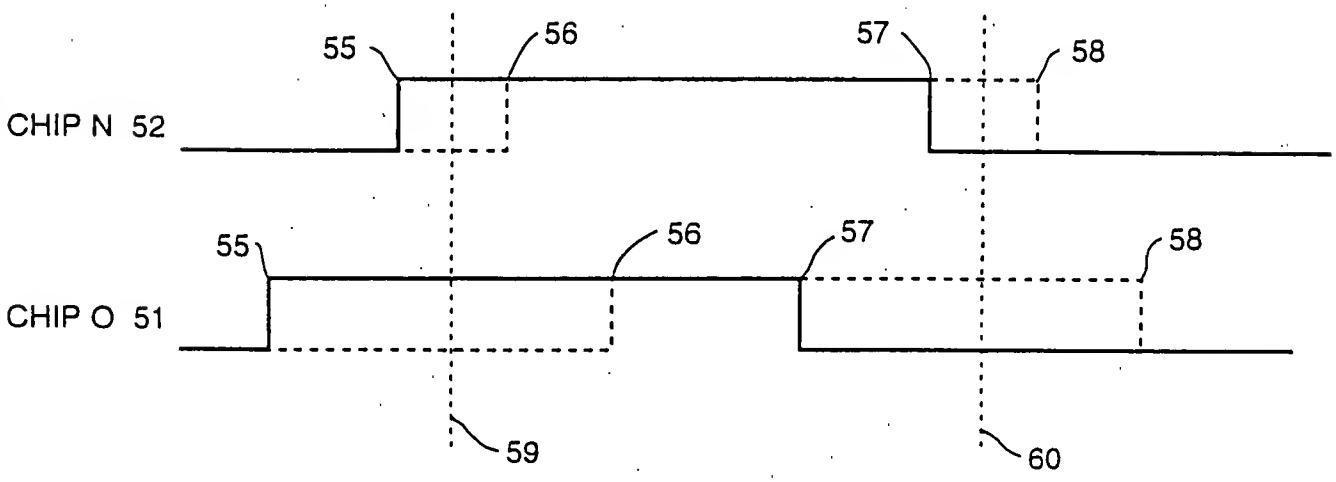


FIG_8B

T0622T "T7E007

FIG_9

T0T22T* T7T7E00T

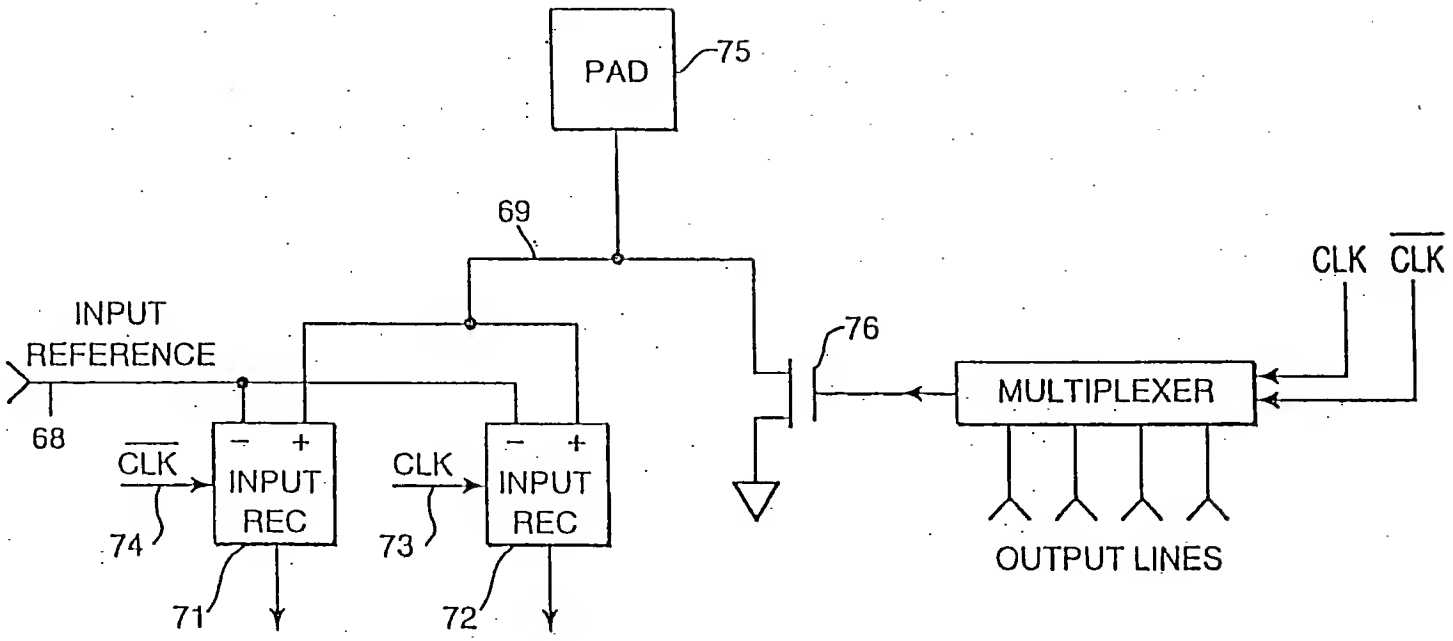
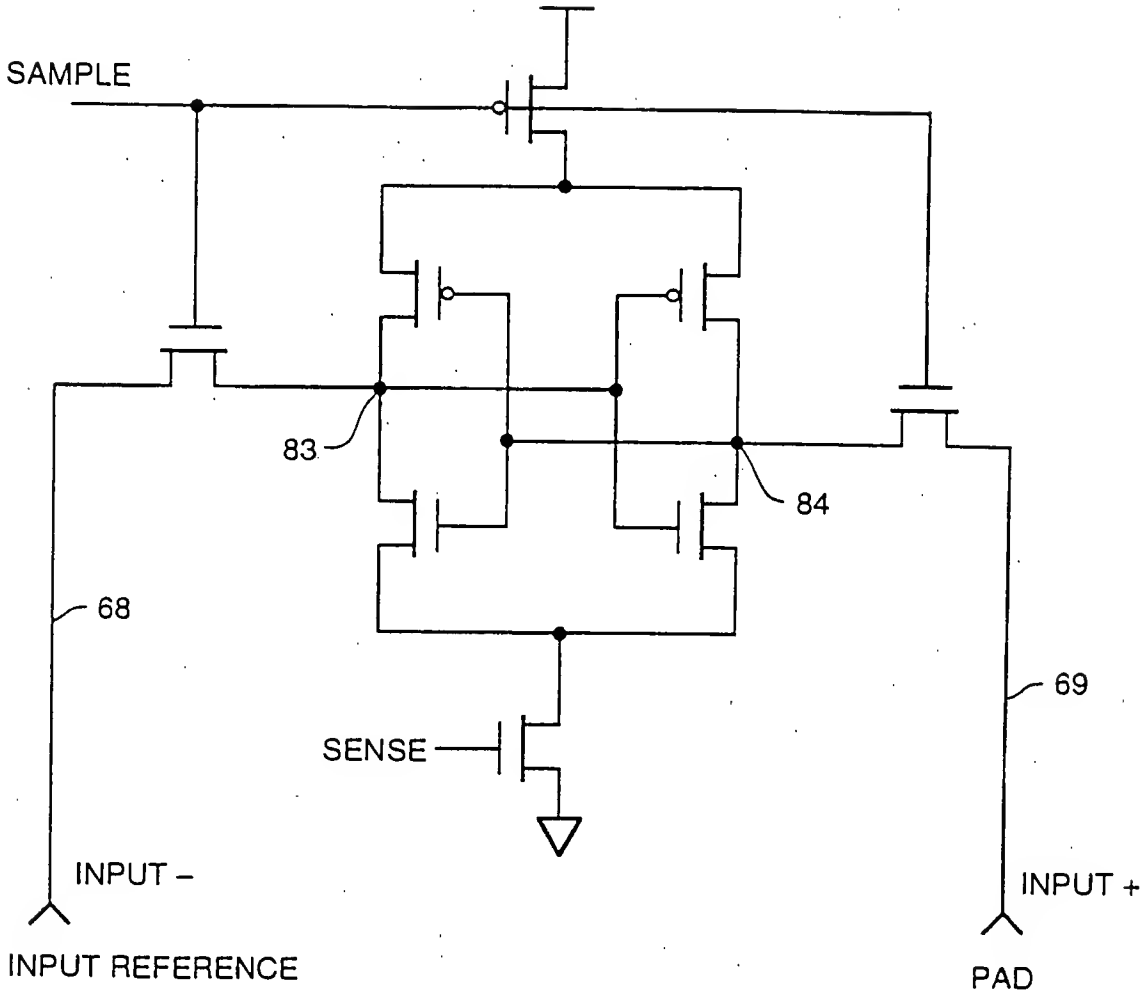


FIG_10

FIG_11



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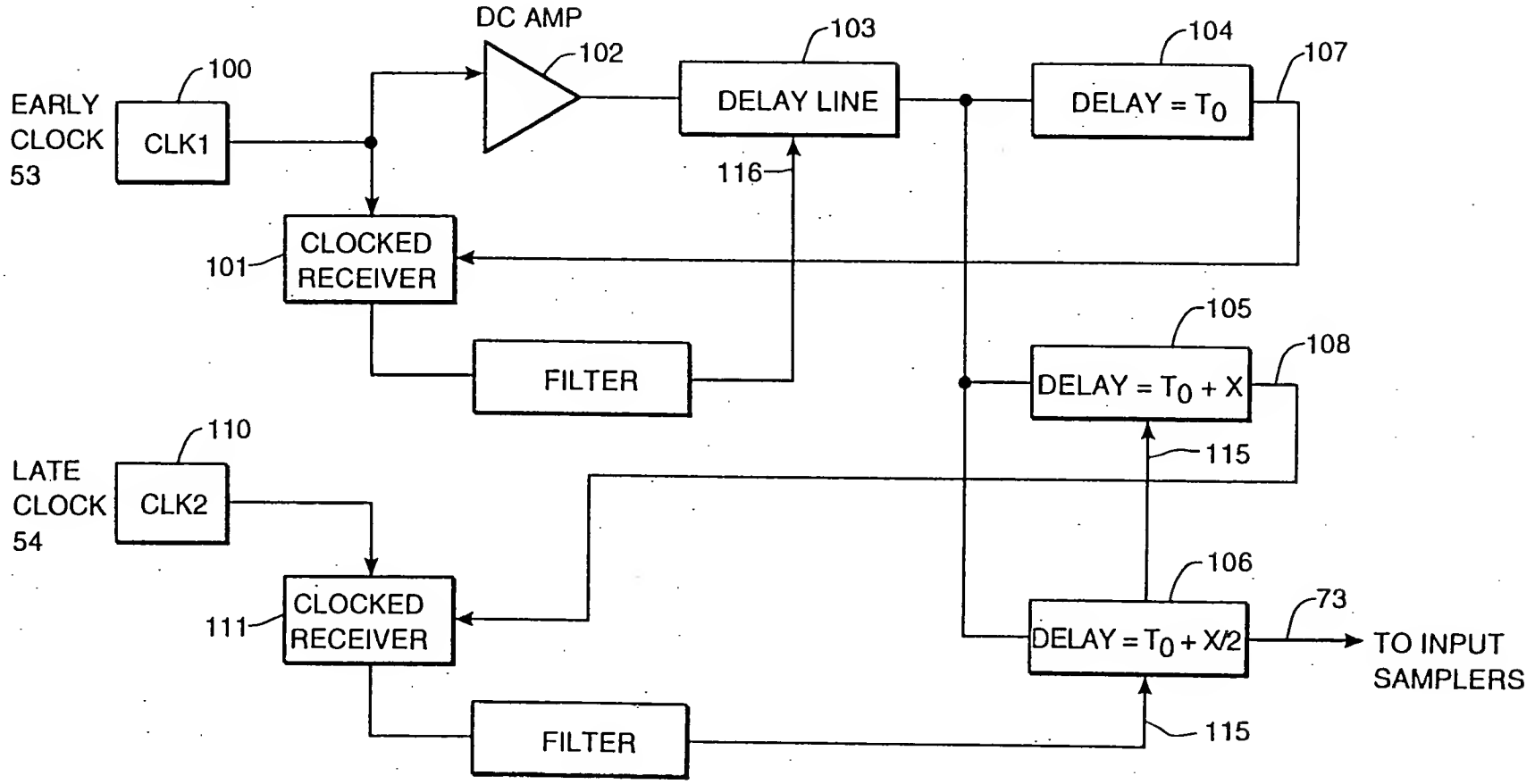
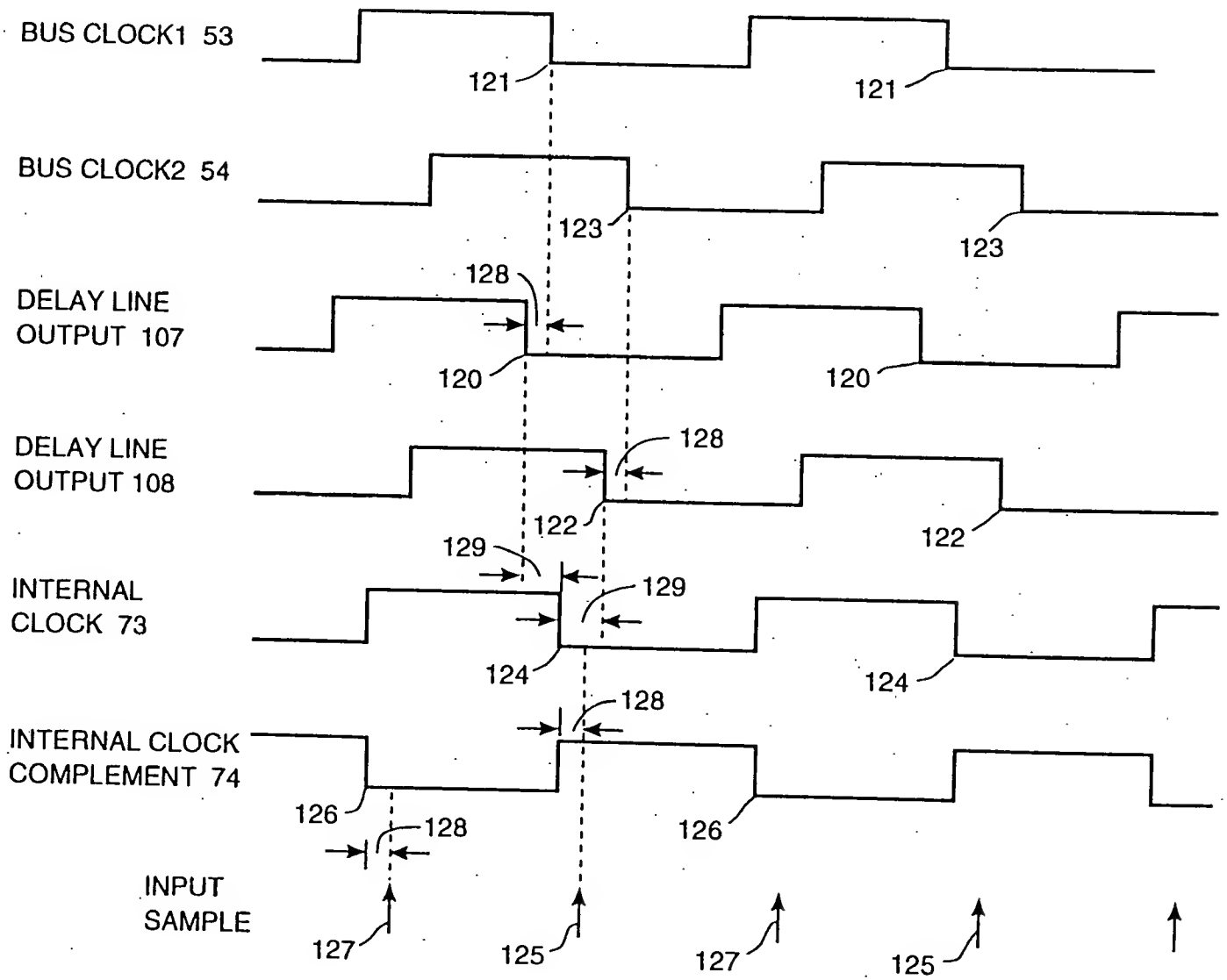
TOP27 P27600T

FIG_12




BUS CLOCK1 53
121
121
BUS CLOCK2 54
123
123
DELAY LINE OUTPUT 107
128
120
120
DELAY LINE OUTPUT 108
128
122
122
INTERNAL CLOCK 73
129
129
124
124
INTERNAL CLOCK COMPLEMENT 74
128
126
126
128
INPUT SAMPLE
127
125
127
125

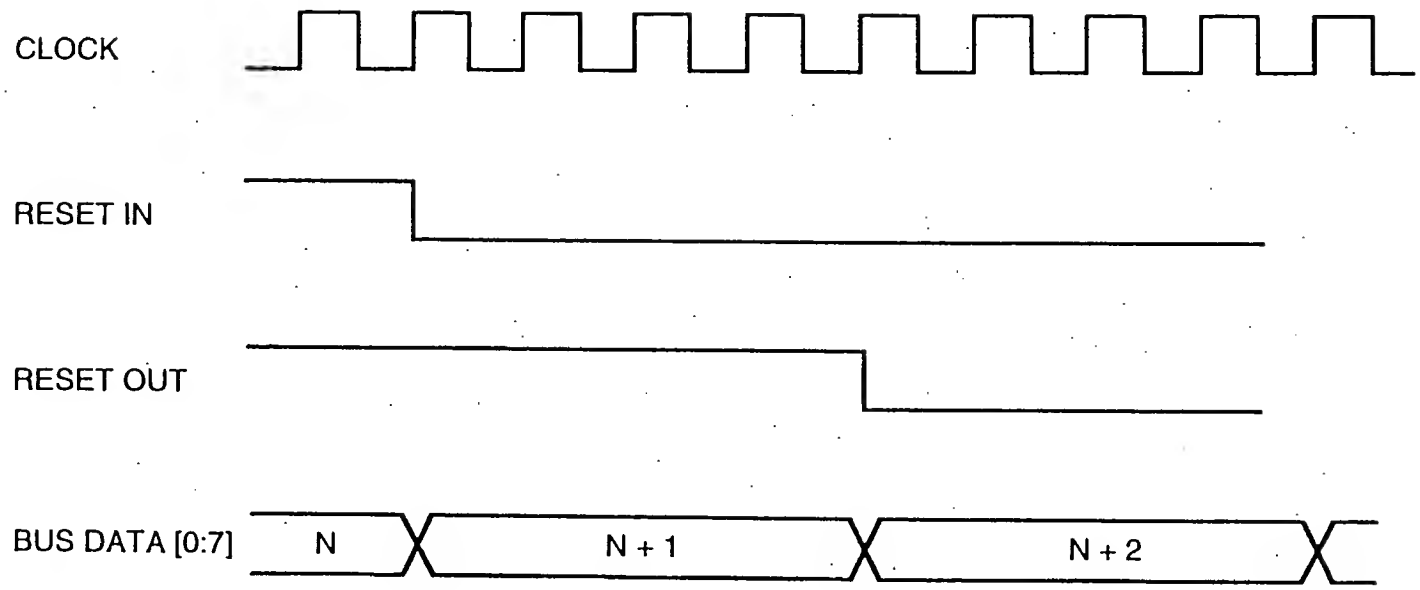
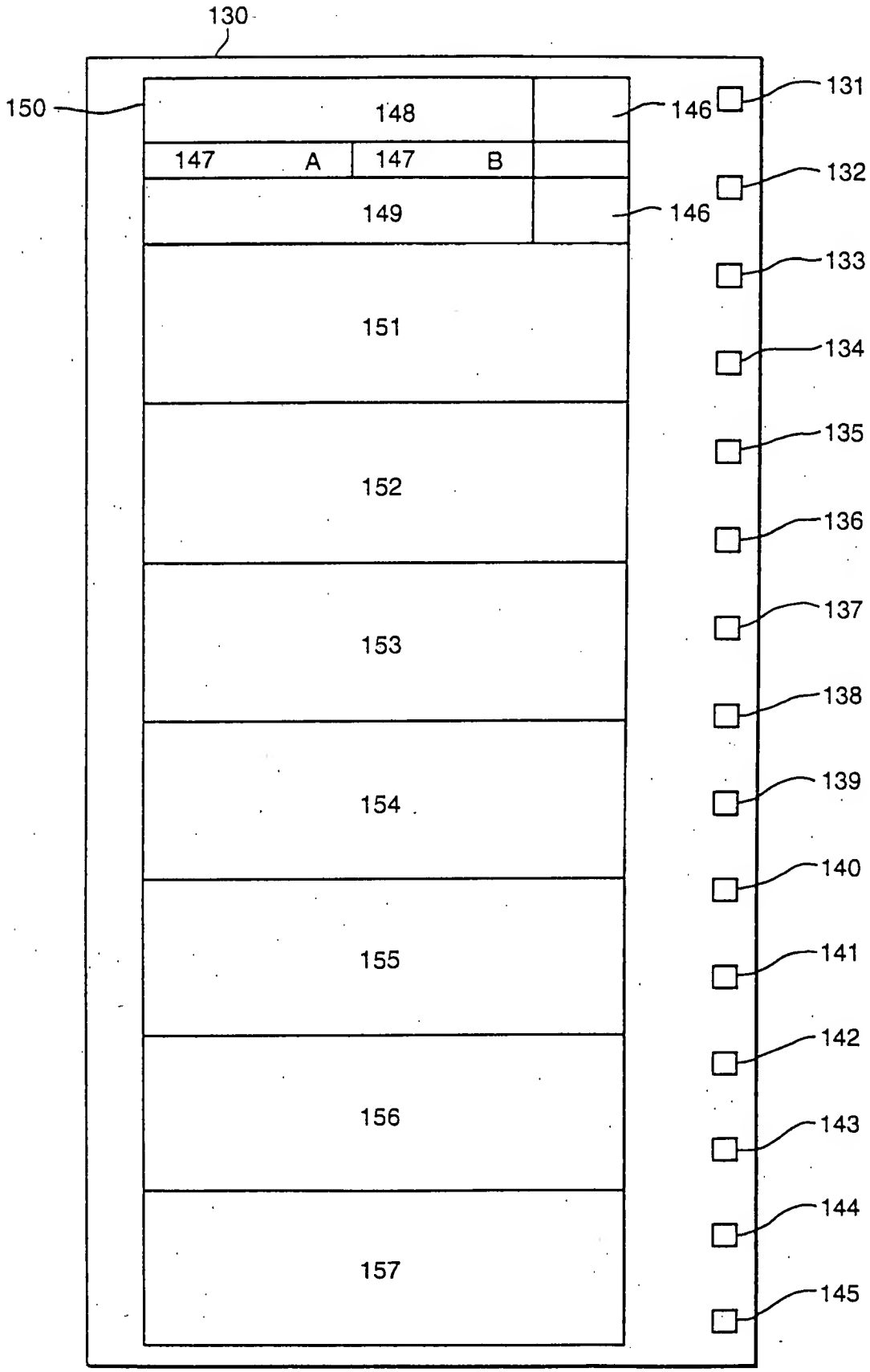


FIG_14

FIG_15


130
150
148
146
131
147
A
147
B
132
149
146
133
151
134
135
152
136
153
137
138
154
139
140
155
141
142
156
143
144
157
145

T0T22T' TZTZE00T

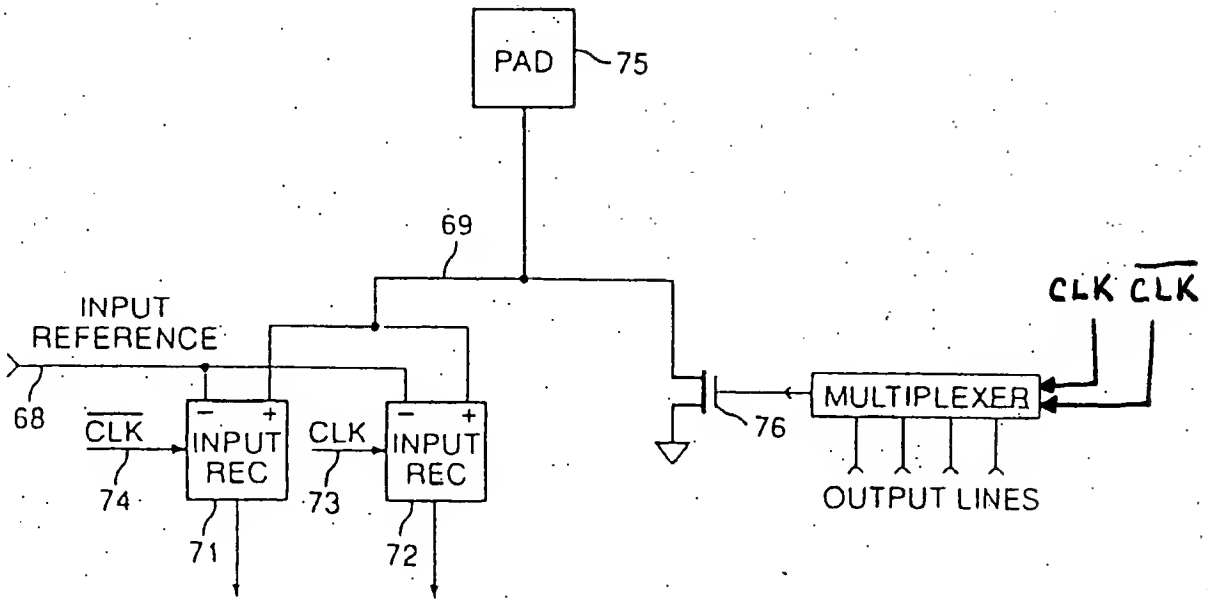


FIG. 10